REMARKS

Reconsideration of the application in view of the above amendments and the following remarks is respectfully requested.

Drawings – Figure 9A has been amended to reflect a feature inadvertently omitted in the figures originally filed. In particular, a silicon oxide layer is now presented on an exposed surface of the substrate 20 directly above silicon channels 54, 53 and 52. This silicon oxide layer is formed simultaneously with the silicon oxide layers (90) of the silicon channels 54, 53 and 52. Accordingly, in the amended Figure 9A, the silicon oxide layer of the silicon substrate directly above the channels is also designated as 90. Support for this amendment can be found on page 8, lines 6-11. One sheet of replacement drawings is submitted herewith for approval.

Claims 1-3 and 9-24 are pending. Claims 1, 3, 11-12 and 19-20 are amended. No new matter is introduced by these amendments.

Claim 1 is rejected under 35 U.S.C 112, second paragraph as being indefinite. The Examiner alleges that with regard to "the silicon surfaces of the active surfaces opposite to the conductive strips and the conductive regions are covered with an insulator forming a gate oxide", it is not clear what or where the silicon surfaces are located in the transistor.

The applicants have amended claim 1. The amended claim 1 is directed to a MOS transistor in a single-crystal silicon substrate. In particular, claim 1 recites a first conductive strip above an upper portion of the single-crystal silicon substrate, a second conductive strip being placed in the upper portion and below the first conductive strip, and conductive regions being placed against ends of the first and second conductive strips, the first and second conductive strips and the conductive regions forming a gate. The claimed structures, i.e., the first conductive strip, the second conductive strip and the conductive regions are formed in or above the single-crystal silicon substrate. Accordingly, the phrase "silicon surfaces abutting the gate" refers unambiguously to the parts of the single-crystal substrate that adjoining the gate structures. The applicants respectfully submit that claim 1, as amended, is not indefinite. The Applicants request that this ground of rejection be withdrawn.

The Examiner has rejected claims 1, 3 and 9-11 as being anticipated by DE 19928564 to Shultz (hereafter "Shultz"). More specifically, the Examiner states that Shultz discloses in Figure 1: a silicon substrate (1), an active area surround by an insulating wall (12), a first conductive strip (10c), a second conductive strip (10a/10b), conductive regions (2a/2b), and gate oxide (9).

Shultz does not disclose the invention recited in claim 1, as amended. Claim 1 as amended is directed to a MOS transistor in a single-crystal silicon substrate. As noted above, claim 1 recites a first conductive strip above an upper portion of the single-crystal silicon substrate, a second conductive strip being placed in the upper portion and below the first conductive strip, and conductive regions being placed against ends of the first and second conductive strips, the first and second conductive strips and the conductive regions forming a gate. The claimed structures are formed within the single-crystal silicon substrate.

The above claimed features are not disclosed or suggested in Shultz. Figure 1 of Shultz describes source and drain regions (2A and 2B), a first gate (10A) and a second gate (10B) formed above an insulating layer (1.2) covering a silicon substrate (1.1). In Shultz, the gates are not in the silicon substrate. Instead, the gates are in contact with two semiconductor channel layers (6A and 4A). These semiconductor channel layers, however, are not part of the single-crystal lattice of the silicon substrate, as they are separated from the silicon substrate (1.1) by an insulator layer (1.2)

Claim 3 is also amended to further clarify the positions of the conductive regions relative to the first and second conductive strips. Claim 3 is also novel over Shultz as it further limits claim 1. For the same reason, claims 9-11 are patentable in view of Shultz.

Relying on the same analysis in rejecting claims 1-3, the Examiner further rejects claims 12, 17-21 as being anticipated by Shultz.

In response, the applicants have amended claim 12. Support for these amendments can be found, e.g., on page 7 and Figures 4A, 5A and 6A. In particular, claim 12 as amended is directed to a MOS transistor formed in a single-crystal silicon substrate. Moreover, claim 12 recites a first conductive strip, a first insulating layer immediately below the first conductive strip, and a second conductive strip separated from a first insulating layer by a single-

crystal silicon layer, the single-crystal silicon layer being a part of the single-crystal of the silicon substrate.

These above features are not described in Shultz. As discussed above, the semiconductor channel layers (4A and 6A) in Figure 1 of Shultz are not part of the crystal lattice of the silicon substrate, because they are separated from the silicon substrate (1.1) by an insulating layer (1.2). The applicants therefore submit that Shultz does not disclose each and every element of claim 12. Claim 12, as well as its dependent claims 17-19, is therefore novel in view of Shultz

Similarly, claims 19-20 have been amended to specify that the single-crystal silicon layers are parts of the single-crystal silicon substrate. Based on the same rationale as set forth above, claims 20-21 are also patentable over Shultz.

The Examiner further rejects claims 2, 13-15 and 22-24 as unpatentable over Shultz in view of U.S. Patent No. 6,396,108 to Krivokapic (hereafter "Krivokapic"). In particular, the Examiner states "Shultz discloses all the limitations except for the conductive strips to be polysilicon." The Examiner further states that Krivokapic discloses a double gate of conductive strips formed of polysilicon. The Examiner therefore concludes that claims 2, 13-15 and 22-24 are obvious to one skilled in the art in view of the combined teachings of Shultz and Krivokapic.

Shultz and Krivokapic do not teach or suggest the invention of claims 2, 13-15 and 22-24. As discussed above, Shultz does not disclose or suggest all the limitations of independent claims 1, 12 and 20. In particular, Shultz does not disclose or suggest that the claimed structures (first and second conductive strips and the conductive regions) are formed within a single-crystal silicon substrate. This deficiency is not cured by Krivokapic. The double gates in Krivokapic are not formed in a single-crystal substrate. Krivokapic therefore does not add anything to the disclosure of Shultz. The applicants therefore respectfully request this ground of rejection be withdrawn.

The Director is authorized to charge any additional fees due by way of this Amendment, or credit any overpayment, to our Deposit Account No. 19-1090.

All of the claims remaining in the application are now clearly allowable. Favorable consideration and a Notice of Allowance are earnestly solicited.

Respectfully submitted,

SEED Intellectual Property Law Group PLLC

Hai Han, Ph.D.
Registration No. 54,150

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Enclosures:
Postcard
One Sheet of Replacement Drawings (Figures 7A-7B, 8A-8B and 9A-9B)

701 Fifth Avenue, Suite 6300
Seattle, Washington 98104-7092
Phone: (206) 622-4900
Fax: (206) 682-6031

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Amendments to the Drawings:

The attached sheet of drawings includes changes to Figure 9A. This sheet, which includes Figures 7A, 7B, 8A, 8B, 9A and 9B, replaces the original sheet including Figures 7A, 7B, 8A, 8B, 9A and 9B.

Attachment: 1 Replacement Sheet